Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A0**
2. **EN**
3. **VSS**
4. **S1**
5. **S2**
6. **S3**
7. **S4**
8. **D**
9. **S8**
10. **S7**
11. **S6**
12. **S5**
13. **VDD**
14. **GND**
15. **A2**
16. **A1**

**7 8 9**

**3 2 1 16 15 14**

**13**

**12**

**11**

**10**

**4**

**5**

**6**

**LOGO**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: H24B**

**APPROVED BY: DK DIE SIZE .069” X .071” DATE: 6/16/22**

**MFG: ANALOG DEVICES THICKNESS .014” P/N: ADG508AB**

**DG 10.1.2**

#### Rev B, 7/19/02